A Capacitor-Fed, Voltage-Step-Down, Single-Phase, Non-Isolated Rectifier

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Abstract — **A simple rectifier, little documented in the literature, provides a low-voltage output from an ac-mains supply, with inherent short-circuit protection. We present waveforms, a theoretical analysis, simulation results (within ±2% of theoretical predictions over a 512:1 range of the principal design parameter) and experimental confirmation, and propose variants with improved regulation. The line-harmonic characteristics comply with IEC 1000-3-2, Class A, at power levels up to 250W. This rectifier finds application in equipment requiring a low-voltage, non-isolated dc supply.**

I. INTRODUCTION

Most equipment operating from the ac power mains needs low voltage dc. Traditionally, the power supply is a 50/60 Hz step-down transformer followed by rectification, or a SMPS comprising a rectifier followed by a step-down dc/dc converter. In either case, it is easy to include isolation.

However, in many applications, electrical isolation of the internal circuitry is unnecessary. Low-power equipment with no user inputs or outputs can use double-insulated enclosures to comply with electrical safety requirements. Examples include clocks, certain battery chargers, and auxiliary supplies for the primary-side control circuits of SMPSs. Television receivers have also used this approach widely. In these applications it is advantageous to use a small, lightweight, low-cost power supply with a low component count. At higher power levels, e.g., for motor drives, the whole equipment may be live, including the output; there is then little virtue in having an isolated auxiliary supply.

Direct rectification normally gives a voltage approaching the peak value of the mains voltage. But an impedance can be placed in series with the ac input to reduce the dc output voltage. If the impedance is resistive, a low efficiency will result; but if it is reactive, the circuit will be essentially lossless (apart from a small power loss in the parasitic series resistance, and diode losses).

Using either a capacitor or an inductor reduces the line-current harmonics below those of a circuit without the series reactance. The choice between an inductor and a capacitor can be made on their relative size, cost, parasitic losses, and availability. An inductor has the advantage of attenuating spikes that might be on the ac input voltage, but the potential disadvantage of overshoot on the dc output voltage at turn-on, resulting from a resonance between the series inductor and the output reservoir capacitor, especially at light load. In general, low-power applications will favor the capacitor, and high-power applications the inductor. This paper treats only the capacitor version of the circuit (Fig. 1) and its variants.

This rectifier is not new; commercial battery chargers have used it since at least the 1970s. But it is little known and poorly understood. To the best knowledge of the three authors and four independent power-electronics consultants, the only published information is brief descriptions in manufacturers' applications notes [1], [2] and a handbook [3] that reprints [2]. Nor does Scoles' encyclopedic compendium of rectifiers [4] contain the circuit. There appears to be no information available on operation, analysis or design. Moreover, considering IEC 1000-3-2 [5] and similar regulations, it is necessary nowadays to investigate the rectifier's line-current harmonic characteristics. This paper aims to remedy these deficiencies.

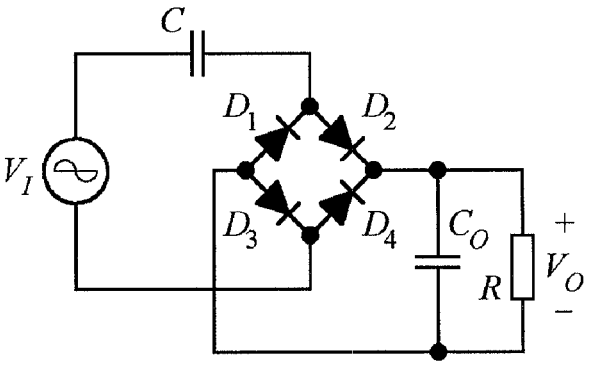

Fig. 1: The capacitor-fed rectifier.

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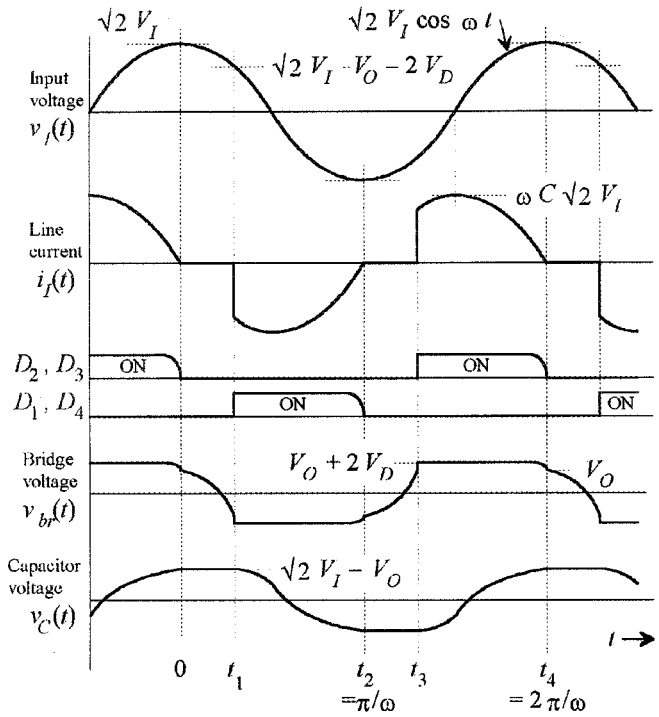

Fig. 2: Waveforms of the capacitor-fed rectifier.

II. CIRCUIT OPERATION AND ANALYSIS

Fig. 1 shows the capacitor-fed rectifier; Fig. 2 shows the circuit's principal steady-state waveforms.

A. Operation

Despite the apparent simplicity of the circuit, the details of its operation are not obvious. The key to understanding is that the series capacitor C operates in a "discontinuous current mode", i.e., its current is zero for part of each half-cycle. Therefore two distinct modes of circuit action occur within each half-cycle.

First, if a pair of bridge diodes is forward-biased, the right-hand terminal of C is clamped to the nearly constant output voltage, while the left-hand terminal follows the sinusoidal input voltage. Because the current through a capacitor is proportional to the rate-of-change of the voltage across it ("$i = C\ dv/dt$"), C passes current. Second, when all the diodes are reverse-biased, no current can flow through C, so the voltage across C must remain constant. This happens for $t = 0$ to t_1 and $t = t_2$ to t_3.

Note that the diodes turn on hard at t_1 and t_3 (i.e., they experience a step increase of current), but turn off softly at t_2 and t_4 (i.e., their current gradually reduces to zero). The consequences of the soft turn-off are discussed under *Interval 2* below.

B. Analysis of Operation

In this analysis we take all components as ideal, except for the diodes, which have a constant forward voltage V_D during conduction. The large reservoir capacitor C_O acts to keep the output voltage V_O nearly constant throughout the cycle. We assume initially that C_O is infinite; subsequently, we apply a ripple correction for C_O's finite capacitance.

Let the ac input voltage be

$$v_I(t) = \sqrt{2}V_I \cos \omega t \tag{1}$$

where V_I is the rms voltage and $\omega = 2\pi f$ is the angular frequency of the ac supply. The operation during a cycle divides into four intervals.

Interval 1: $0 \le t < t_1$

Consider the half-cycle commencing at $t = 0$. The input voltage is at its peak, where $dv_I/dt = 0$, so no current flows through C. Therefore at $t = 0$, diodes D_2 and D_3 cease conducting. The series capacitor C is left charged to a certain positive voltage. With some prescience, we take this as

$$v_C(0) = \sqrt{2}V_I - V_O \tag{2}$$

a value that will be verified when we reach (11) below. C maintains its voltage at this value as the input voltage starts to fall, because no current flows. Consequently, the diode-bridge input voltage v_{br} falls with the input voltage, and is given by

$$v_{br}(t) = V_O - \sqrt{2}V_I(1 - \cos \omega t) \tag{3}$$

This action continues until v_{br} reaches $-(V_O + 2V_D)$, when D_1 and D_4 become forward-biased, at t_1. Then

$$v_{br}(t_1) = V_O - \sqrt{2}V_I \cos \omega t_1 = -(V_O + 2V_D) \tag{4}$$

Hence

$$\cos \omega t_1 = 1 - \frac{\sqrt{2}(V_O + V_D)}{V_I} \tag{5}$$

Interval 2: $t_1 \le t < t_2$

At t_1, D_1 and D_4 start to conduct, clamping the right-hand terminal of C to $-(V_O + 2V_D)$. The left-hand terminal is connected to v_I, so the overall voltage across C is

$$v_C(t) = \sqrt{2}V_I \cos \omega t + V_O + 2V_D \tag{6}$$

Its current is therefore

$$i_I(t) = \frac{dv_C}{dt} = -\omega C \sqrt{2} V_I \sin \omega t \tag{7}$$

So at t_1, current suddenly starts flowing through C, at a value determined by the rate-of-change of the input voltage; from (5) and (6),

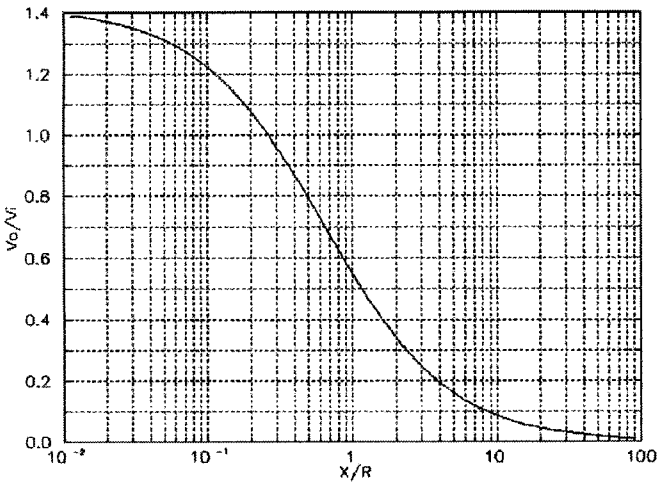

Fig. 3: Plot of X/R as a function of V_O/V_I, with $V_D = 0$. Increasing the series capacitive reactance reduces the output voltage.

$$i_I(t_1) = -\omega C\sqrt{2}V_I \sin\left[\cos^{-1}\left(1-\frac{\sqrt{2}(V_O - V_D)}{V_I}\right)\right] \qquad (8)$$

This is a hard turn-on, and the voltage of D_1 and D_4 each jumps to V_D as they start to conduct.

Thereafter during this interval, the current $i_I(t)$ leads the voltage $v_I(t)$ by 90 ° until, at $t_2 = \pi/\omega$, the input voltage reaches its most negative, dv_I/dt becomes zero, and the current also goes to zero. From (6) we would expect

$$v_C(t_2) = -\sqrt{2}V_I + V_O + 2V_D \qquad \text{(wrong!)} \ (9)$$

However, from the current waveform it is apparent that this is a soft turn-off, the current reducing slowly to zero. So, at t_2, the conduction voltage of each diode is more accurately taken as zero, not V_D. Therefore, instead of (9), we write

$$v_C(t_2) = -\sqrt{2}V_I + V_O \qquad (10)$$

For a real diode, the conduction voltage is around 0.8 V, drooping to about 0.2 V as the current drops to zero, then rapidly reverses as any remnant charge is swept out. This is verified by simulation. (The reverse recovery time and recovered charge are, however, negligible in this context.) The important point is that C is charged to the voltage in (10), to a close approximation, and stores it throughout Interval 3.

Interval 3: $t_2 \le t < t_3$; Interval 4: $t_3 \le t < t_4$

Intervals 3 and 4 are similar to Intervals 1 and 2 respectively, but with reversed currents and voltages. At $t_4 = 2\pi/\omega$, the voltage across C is (employing (10) with a change of sign):

$$v_C(2\pi/\omega) = \sqrt{2}V_I - V_O \qquad (11)$$

Thus the capacitor voltage at the end of the cycle is the same as that at the beginning (see (2)), verifying that this is, indeed, the steady state.

C. Rectifier DC Characteristics

Having obtained expressions for the waveforms, we can now find some characteristics of the rectifier.

Integrating over a half-cycle of the input yields the rectified-mean input current, which is equal to the mean (dc) output current I_O. Thus

$$I_O = \frac{\omega}{\pi}\int_{t_2}^{t_4} i_I(t)\,dt = 4fC\left(\sqrt{2}V_I - V_O - V_D\right) \qquad (12)$$

(Because the circuit uses a diode bridge in which pairs of diodes conduct in series, one might expect that (12) would contain the term $2V_D$. Instead, V_D appears. An explanation follows from the diode switching. Although the turn-on at t_3 is hard, and the total conduction drop is $2V_D$ at that point, the turn-off at t_4 is soft, and the diode drops are taken as zero. The effect of (12) is to take the average, producing a single V_D.)

Let the magnitude of the capacitive reactance at ω be

$$X \triangleq \left|\frac{-1}{\omega C}\right| = \frac{1}{\omega C} \qquad (13)$$

(Capacitive reactance is actually negative. We employ the notation X for convenience throughout this paper, to avoid writing $|X|$ continually.)

Using (12) and the fact that $V_O = I_O R$, we find the rectifier's dc output voltage as

$$V_O = \frac{2R}{\pi X}\cdot\frac{\sqrt{2}V_I - V_D}{1+\frac{2R}{\pi X}} \qquad (14)$$

The output voltage depends on the amount of capacitive reactance present, normalized with respect to the load resistance, i.e., X/R is the main design parameter. With $X/R \ll 1$, the output voltage approaches the peak value of the input voltage, as expected; when $X/R \gg 1$, the output voltage is low. We rearrange (14) into the form

$$X = \frac{2R}{\pi}\cdot\frac{\sqrt{2}V_I - V_O - V_D}{V_O} \qquad (15)$$

Assuming $V_D \ll V_I$, Fig. 3 shows a dimensionless plot of X/R versus V_I/V_O, which can be used for design purposes.

Equation (12) can be rearranged to give the dc output characteristic:

$$V_O = \sqrt{2}V_I - V_D - \frac{I_O}{4fC} \quad \text{if } I_O > 0 \qquad (16)$$

Thus the rectifier may be represented by a Thevenin equivalent comprising a voltage source of $\sqrt{2}V_I - V_D$ in series with a resistance of $1/4fC$. (This resistance is lossless, because it is actually due to capacitive reactance on the ac side of the rectifier.)

Putting $I_O = 0$ in (16), the open-circuit voltage is found as

$$V_{O(\text{open})} = \sqrt{2}V_I \tag{17}$$

On the other hand, setting $V_O = 0$ yields the short-circuit output current as

$$I_{O(\text{short})} = \sqrt{32}fCV_I \tag{18}$$

Thus the rectifier has the useful feature of inherent overload protection. The rectifier now appears to the ac supply as a simple capacitive reactance, and the rms line current is

$$I_{I(\text{short})} = 2\pi fCV_I \tag{19}$$

If $V_O << V_I$, the rectifier approximates a dc current source. This makes it useful for applications such as constant-current charging of nickel–cadmium batteries [1], the battery replacing C_O and R.

D. Correction for Finite Output Capacitance

The actual output voltage will be lower than the value predicted using $C_O = \infty$, due to the presence of ripple. Assuming that the ac ripple waveform is symmetrical about the mean output voltage level, we can multiply V_O by a ripple correction:

$$V_{O(\text{corrected})} = V_O(1 - r/2) \tag{20}$$

where the ripple factor r is defined in terms of ΔV_O, the peak-to-peak output voltage ripple, as

$$r = \frac{\Delta V_O}{V_{O(\text{corrected})}} \tag{21}$$

It seems reasonable that r should be inversely proportional to f, C_O and R, at least to a first approximation. In reality, r also varies with X/R, because the conduction angle of the diodes changes. Taking this approach, we can estimate the value of r from

$$r \approx \frac{0.24 - 0.10\log_{10}(X/R)}{fC_OR} \tag{22}$$

which we obtained by a combination of analysis and fitting a function to values of r obtained by PSpice simulation, for $0.03125 \le X/R \le 16$. We plan to investigate the ripple correction theoretically in a future paper.

TABLE I: OUTPUT VOLTAGE, BY THEORY AND SIMULATION

	V_O		Discrepancy	
X/R	Theoretical* (V)	Simulation (V)	Absolute (V)	Relative (%)
0.03125	155.76	153.12	2.64	1.7
0 0625	149.19	147.50	1.69	1.1
0.125	137.30	137.00	0.30	0.2
0.25	118.25	118.00	0.25	0.2
0.5	92.47	92.95	–0.48	–0.5
1	64.39	65.15	–0.76	–1.2
2	40 07	40 55	–0.48	–1.2
4	22 84	23 12	–0 28	–1.2
8	12 30	12.38	–0.08	–0.6
16	6.40	6.46	–0.06	–0.9

* Calculated from (20)

III. SIMULATION RESULTS

We ran a series of PSpice simulations to verify the analysis. The parameter values were V_I = 120 Vrms, f = 60 Hz, R = 100 Ω and C_O = 1 mF. The value of C varied among runs. Each diode employed the default SPICE model, its series resistance being set to 0.5 Ω. Table I compares the steady-state output voltage to the theoretical predictions obtained from (14), using V_D = 0.8 V and the ripple correction of (22).

The theoretical and simulation results agree well, to better than ±2% over the 512:1 range of X/R. The discrepancy is greatest at low X/R (approaching a conventional rectifier). The reason is that the input current has a very spiky waveform, causing a significant voltage across the diodes' ohmic series resistance, which was excluded from the analysis. This is of little consequence, though, as the rectifier is intended mainly for step-down applications, where X/R is high.

IV. DESIGN PROCEDURE AND CONFIRMATION

A. Design Procedure

The design of the rectifier can proceed as follows:

1. Represent the dc load as an equivalent resistance $R = V_{O(\text{corrected})}/I_O$, where $V_{O(\text{corrected})}$ is the desired dc output voltage.

2. Define a desired ripple factor r from (21).

3. Find the infinite-C_O output voltage $V_O = V_{O(\text{corrected})}/(1 - r/2)$.

4. Use (15) to find X. (Or, less accurately, obtain X/R from Fig. 3 and multiply by R.) Then $C = 1/2\pi fX$.

5. Use (22) to calculate the needed output smoothing capacitance C_O.

6. Find the short-circuit output current from (18).

Design Example

Given: V_I = 230 V, f = 50 Hz, $V_{O(\text{corrected})}$ = 12 V with 0.5 V peak-to-peak ripple superimposed, at I_O = 1 A. Find component values for the rectifier.

1. Dc load resistance $R = 12/1 = 12\ \Omega$.

2. Ripple factor $r \approx 0.5/12 = 0.042$.

3. Infinite-C_O output voltage $V_O = 12/(1 - 0.042/2) = 12.26$ V.

4. A suitable diode bridge has $V_D = 0.85$ V. Then $X = 2 \times 12.26 / \pi \times (\sqrt{2} \times 230 - (12.26 + 0.85)) / 12 = 199\ \Omega$. So $C = 1 / (2\pi \times 50 \times 199) = 16.0\ \mu F$.

5. Output capacitance $C_O = (0.24 - 0.10 \log_{10} (199/12)) / (50 \times 12 \times 0.042) = 4.68$ mF.

6. The short-circuit output current is $\sqrt{32} \times 230 \times 50 \times 16.0 \times 10^{-6} = 1.04$ A, only 4% higher than the nominal current in normal operation.

B. Confirmation by Simulation and Experiment

The design was constructed with measured values of $C = 15.75\ \mu F$ (nominally $2 \times 8\ \mu F$, 440 V ac, metallized polypropylene film), $V_D = 0.85$ V at 1 A dc (GBPC106 diode bridge: 600 V, 2 A), and $C_O = 5.83$ mF (nominally 4.7 mF, 63 V dc, electrolytic). Its performance was measured using a power amplifier to deliver an undistorted 230 V, 50 Hz sine wave, with a rheostat as the dc load. The design was also analyzed and simulated using the measured values. Table II compares the three sets of results, which agree well over a wide range of output voltage.

TABLE II: COMPARISON OF EXPERIMENTAL, ANALYTICAL AND SIMULATION RESULTS

	Experiment	Analysis	Simulation
$R = 0.11\ \Omega$ (short circuit):			
V_O (V)	0.11	0 00 *	0.11
I_O (A)	1.01	1.02 *	1.03
ΔV_O (Vpk-pk)	—	—	0.15
$R = 6\ 06\ \Omega$:			
V_O (V)	6.00	5.93	6.08
I_O (A)	0.99	0.98	1.00
ΔV_O (Vpk-pk)	0.44	0.29	0.39
$R = 12.37\ \Omega$ (design point):			
V_O (V)	12.00	11.97	12.16
I_O (A)	0.97	0.97	0.98
ΔV_O (Vpk-pk)	0.44	0.39	0.41
$R = 18.75\ \Omega$:			
V_O (V)	18.00	17.87	18.11
I_O (A)	0.96	0.95	0.97
ΔV_O (Vpk-pk)	0.44	0.45	0.43
$R = 25.53\ \Omega$:			
V_O (V)	24.00	23.90	24.14
I_O (A)	0.94	0.94	0.95
ΔV_O (Vpk-pk)	0.50	0.48	0.45
$R = 32\ 26\ \Omega$:			
V_O (V)	30.00	29.67	29.94
I_O (A)	0.93	0.92	0.93
ΔV_O (Vpk-pk)	0.50	0.51	0.47

I_O = output current, V_O = output voltage, ΔV_O = output voltage ripple
R calculated from V_O/I_O using experimental values
* Assuming $R = 0$ and $V_D = 0$

V. INPUT-CURRENT HARMONICS

The line-current waveform of the capacitor-fed rectifier is smoother than that of a conventional rectifier, so one might expect the harmonics to be lower. Preliminary PSpice simulation results showed that, indeed, the larger the value of X/R, the lower the harmonic distortion. This is a valuable property, since the rectifier is intended for low output voltages.

Harmonic current emissions from electronic equipment were originally specified in IEC 555-2 (1987), later subsumed within the electromagnetic compatibility standard IEC 1000-3-2:1995. As EN 61000, this European Standard now carries the force of law within Europe. It is therefore important to examine the present rectifier to see whether it can comply.

A. Analysis

In this section we assume ideal diodes, i.e., $V_D = 0$, and an infinite output capacitance, i.e., $C_O = \infty$. The shape of the input current waveform, $i_I(t)$, is identical to that of a phase-controlled triac with a resistive load (though its relation to the supply voltage is different). That case is analyzed in [6]. The rms input current is

$$I_I = I\sqrt{1 - \frac{2\alpha - \sin 2\alpha}{2\pi}} \tag{23}$$

where $I = I_{I(\text{short})}$, see (19), and $\alpha = \omega t_1$. Equations (5) and (14) give α as

$$\alpha = \cos^{-1}\left(1 - \frac{4R}{\pi X} \cdot \frac{1}{1 + 2R/\pi X}\right) \tag{24}$$

Textbooks find the harmonic structure of the triac's current by Fourier analysis. Unfortunately, we found that some contain incorrect formulae (despite correct accompanying graphs!). Using the Maple V symbolic algebra package, we found the rms value of the fundamental to be

$$I_{I(1)}(\alpha) = \frac{I}{\pi}\sqrt{\frac{1 + 2(\pi - \alpha)^2 + 2(\pi - \alpha)\sin 2\alpha - \cos 2\alpha}{2}} \tag{25}$$

The input current contains only odd harmonics, due to the waveform's symmetry. Harmonic currents for $n = 3, 5, 7, 9, \ldots$ are given by

$$I_{I(n)}(\alpha) = \frac{2I}{\pi(n^2 - 1)}\sqrt{\begin{matrix}1 + n^2 - (n^2 - 1)\cos^2\alpha \\ -2(\cos\alpha\cos n\alpha + n\sin\alpha\sin n\alpha)\end{matrix}} \tag{26}$$

The third harmonic dominates, irrespective of α.

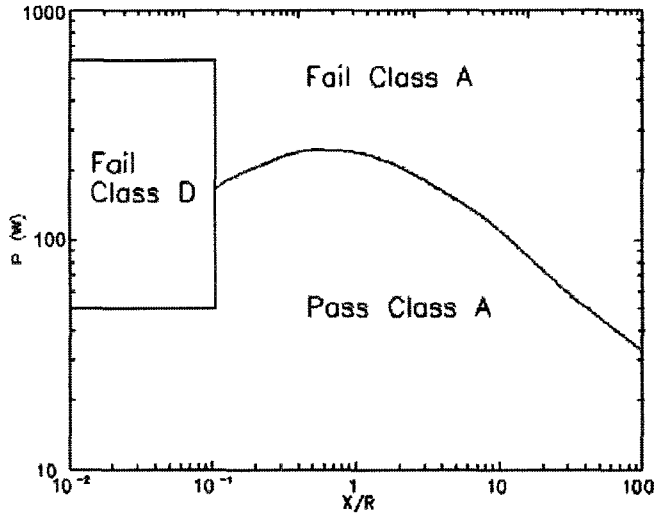

Fig. 4: The *X/R–P* parameter plane, showing IEC 1000-3-2 classes and pass/fail regions.

We now set these results within the context of IEC 1000-3-2. Two classes of equipment are relevant to rectifiers. If a rectifier's active power consumption is from 50 W to 600 W and its line-current waveform fits within a given template, it belongs to Class D. Otherwise, it belongs to Class A. Different harmonic limits apply for each category, Class D being the stricter. (The 50 W lower limit applies from July 1998; prior to that, it is 75W.)

With a sinusoidal voltage, the only contribution to active power consumption is from the in-phase component of fundamental current. The active power consumption of the rectifier is therefore

$$P = V_I I_{I(1)} \cos\phi_1 \tag{27}$$

where ϕ_1 is the phase angle between V_I and $I_{I(1)}$. Further, since we take the diodes as ideal, the input power equals the output power. Hence

$$P = V_O I_O \tag{28}$$

The design example of Section IV has X/R = 199/12 = 16.6, so $\alpha = 0.387$ and the input current is 1.14 Arms. The output power is 12 W, so the power factor is approximately 12/(230 × 1.14) = 0.045. The extremely low power factor is due to the series capacitor, not harmonic currents: the total harmonic distortion is only 9.5%. This rectifier's leading displacement factor (cos ϕ_1) can assist in compensating for lagging displacement factors elsewhere.

B IEC 1000-3-2, Class D

To see whether the rectifier will comply with IEC-1000-3-2, we first examine its power consumption, P. If 50 W ≤ P ≤ 600 W we try the input current waveform against the Class D template, which is specified by three segments:

$$i_I(\omega t) \le \begin{cases} 0.35 I_{pk} & \text{if } 0 \le \omega t < \pi/3 \\ I_{pk} & \text{if } \pi/3 \le \omega t < 2\pi/3 \\ 0.35 I_{pk} & \text{if } 2\pi/3 \le \omega t < \pi \end{cases} \tag{29}$$

For the purposes of this trial, the current's time origin, $t = 0$, is adjusted so i_I reaches its peak value, I_{pk}, at the center of the middle segment, i.e., at $\omega t = \pi/2$.

It is easy to show that α must exceed $\pi/2$, and clearly α must be less than π. We find the critical value, α_c, by solving

$$0.35 \sin\alpha_c = \sin(\alpha_c + \pi/6), \quad \pi/2 < \alpha_c < \pi \tag{30}$$

This transcendental equation has the numerical solution α_c = 2.372, or about 136 °. For $\alpha \ge \alpha_c$, the waveform fits within the template. From (5), the condition corresponds to

$$\frac{V_O}{V_I} \ge \frac{1-\cos\alpha_c}{\sqrt{2}} = 1.215 \tag{31}$$

and, using (14),

$$\frac{X}{R} \le \frac{2}{\pi} \cdot \frac{1+\cos\alpha_c}{1-\cos\alpha_c} = 0.104 \tag{32}$$

IEC 1000-3-2 specifies limits for all odd harmonics up to the 39th. Let us examine just the third harmonic. The Class D limit for the third harmonic is 3.4 mA/W, i.e.,

$$I_{I(3)} < 0.0034P \tag{33}$$

It can be shown that (33) can be expressed in the form

$$0.0136 V_I \sin^2\alpha - \sqrt{10 - 8\cos^2\alpha - 2\cos\alpha\cos 3\alpha + 3\sin\alpha\sin 3\alpha} > 0 \tag{34}$$

With V_I = 230 V rms, the European nominal voltage, we find that (34) is never satisfied for 2.372 < α < π. (It is satisfied for the trivial case of $\alpha = \pi$.) Therefore, taking only the third harmonic, we see that the Class D limits are always violated for any valid combination of P and X/R.

C. IEC 1000-3-2, Class A

For parameter values where the rectifier does not fall into Class D, it must be evaluated according to Class A. Fortunately, Class A has absolute (rather than relative) harmonic current limits, and this favors low-power equipment. Taking V_I = 230 V rms, we have calculated each of the odd harmonic currents up to the 39th, for various combinations of P and X/R, and compared them to the published limits. We find that the rectifier will comply with the Class A requirements over a useful range of power. When X/R = 0.104, power up to 65 W is available, rising to a maximum of 250 W when $X/R \approx 0.5$ ($V_O \approx 180$ V), and tailing off again at high values of X/R. Fig. 4 shows the class and pass/fail re-

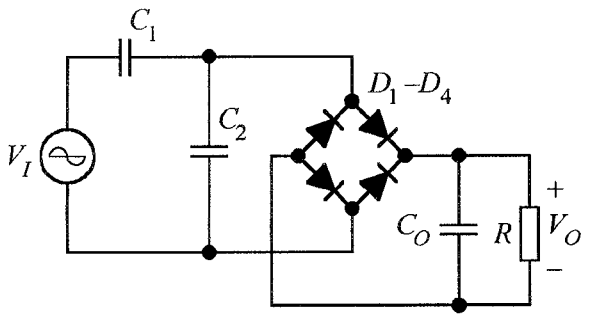

Fig. 5. Use of a capacitive voltage divider (by adding C_2) to reduce the no-load output voltage.

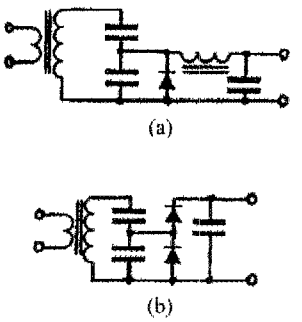

Fig. 6: Two capacitive-divider rectifiers, from Scoles (1980) [4].

gions in the *X/R–P* parameter plane.

These parameters can be interpreted into output current and voltage. For example, to obtain a 5 V dc output from a 230 V supply, X/R = 41. Fig. 4 shows that up to 50 W is available, i.e., an output current of 10 A.

In summary, the rectifier cannot comply with IEC 1000-3-2, Class D. However, for significant voltage step-down ratios, the rectifier falls into Class A. It then meets IEC 1000-3-2 for power levels up to 250 W, depending on the voltage step-down ratio.

VI. CAPACITIVE VOLTAGE DIVISION TO IMPROVE VOLTAGE REGULATION

With the dc load disconnected, the rectifier's output voltage rises to the peak value of the input voltage. This could damage C_O and the diodes, if they are chosen on the basis of the rated output voltage. Moreover, if the load is reconnected it will momentarily experience the full voltage, which could easily result in catastrophic failure.

This problem is reduced in the circuit of Fig. 5, where C_1 and C_2 form a voltage divider. Because both arms of the divider are reactive, efficiency remains high: 100% with ideal components.

A simple approach to analysis is to represent V_I, C_1 and C_2 by a Thevenin-equivalent network, comprising a voltage source V_I' in series with an effective capacitance C, where

$$V_I' = V_I \frac{C_1}{C}, \quad C = C_1 + C_2 \tag{35}$$

This new V_I' and C can be used in the earlier design procedure.

As an illustration, let us modify the design of Section IV to limit its maximum output voltage to 24 V. Step 4 of the design procedure becomes $X = 2 \times 12.26 / \pi \times (24 - (12.26 + 0.85)) / 12 = 7.08\ \Omega$. So C = 450 μF. From (35), $C_1 = CV_I'/V_I$ = 33.2 μF. Hence $C_2 = C - C_1$ = 417 μF. At step 5, the output capacitance becomes $C_O = (0.24 - 0.10 \log_{10} (7.08/12)) / (50 \times 12 \times 0.042)$ = 10.4 mF. The modified Thevenin equivalent of the rectifier's output comprises a 23.15 V dc source in series with a resistance of $1/4fC$ = 11.1 Ω, giving much better voltage regulation than the original design. For example, at a load of 0.5 A, the calculated voltage rises to $23.15 - 0.5 \times 11.1$ = 17.6 V, instead of 168 V.

The short-circuit output current is now 23.15/11.1 = 2.09 A, double that of the original. Because C_2 is itself effectively shorted-circuited via the diode bridge, the input current under these conditions is given by

$$I_{I(\text{short})} = 2\pi f C_1 V_I \tag{36}$$

and here this evaluates to 2.40 A.

PSpice simulation confirms the validity of this design. Probably the main drawback is the increased number and size of the capacitors, though this may not be important at very low power levels.

The technique of capacitive voltage division for rectifiers has been suggested before, but seems to be little used. Scoles [4] briefly described two related circuits, reproduced here as Fig. 6(a) and (b). From Scoles's qualitative description of their operation — there is hardly any analysis — it appears that the two capacitors in Fig. 6(a) act as a voltage divider, while the diode and their combined capacitance form a clamp. In Fig. 6(a) the dc component of the resulting waveform is used. In Fig. 6(b) the second diode and the output capacitor act as a peak rectifier, producing a voltage-doubling effect. In both circuits, it seems that any substantial capacitive reactance would represent a hindrance, rather than being an essential requirement as in our proposed voltage-divider circuit.

VII. PRACTICAL CONSIDERATIONS

As mentioned in Section VI, if the circuit does not use C_2 as in Fig. 5, a large overvoltage can occur when the load is disconnected. In lieu of using C_2, a zener diode or metal-

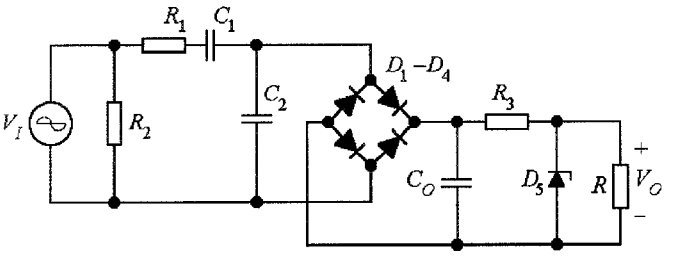

Fig. 7: Some practical improvements to the rectifier.

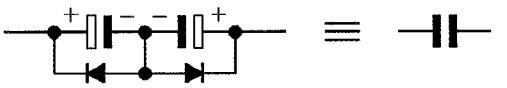

Fig. 8: Two electrolytic capacitors and two diodes can be used to emulate an ac-rated capacitor.

oxide varistor can be connected across the dc output to provide voltage limiting. The breakdown voltage should be somewhat larger than the normal maximum voltage.

Going one step further, a shunt regulator (e.g., R_3 and D_5 in Fig. 7) can give a stabilized output voltage. In this case the breakdown voltage should equal the desired output voltage, and X should be low enough to maintain current through the zener under all conditions.

For small values of series capacitance C (up to perhaps several microfarads), film or ceramic capacitors are convenient. For higher values, electrolytic capacitors will usually be smaller and less costly. When using polarized types, two capacitors must be connected back-to-back shunted by anti-parallel diodes, as in Fig. 8, to prevent reverse voltage. The capacitors' ripple-current rating should be at least equal to the largest ac-line current to be carried, e.g., the current with the load short-circuited.

However, for safety and reliability, C should be a Class X capacitor (i.e., rated for continuous ac-line operation) because it is effectively connected across the line if the output is short-circuited or at a low voltage. Suitable dielectrics include polypropylene film and paper, as used in motor-run and lighting-ballast capacitors, for example. Fast voltage transients will cause high currents to flow through C, so it is beneficial to place a small resistance in series as a current-spike limiter (R_1 in Fig. 7). A value of $X/10$ will usually suffice. The cost is lower efficiency, because power of $I_I^2 R_1$ is dissipated. (Recall that I_I is the rms value of the input current, which, due to its waveform, is higher than the output dc.)

If the power plug is pulled from the ac wall outlet while the rectifier is operating, C can retain energy that depends on the on the line-voltage phase at the moment of disconnection. A person touching the power plug might receive an electric shock. A high-value bleed resistor connected across the rectifier's ac input (R_2 in Fig. 7) will avoid this. The time constant CR_2 should be small, under a second, say. Again, the resistor reduces efficiency, dissipating power of V_I^2/R_2. Alternatively (if the C_1–C_2 divider is not used), R_2 can be placed in parallel with C, reducing the power in R_2 somewhat.

The designer should also note that the rectifier is frequency-sensitive, so care should be taken when designing equipment to be used at both 50 Hz and 60 Hz.

VIII. CONCLUSION

The paper describes a simple, useful rectifier that is little documented in the literature. It features voltage step-down operation, acceptable line-current harmonics, inherent short-circuit protection and, optionally, a regulated output. However, it is limited to applications where input-isolation is not required.

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