

Application Note AN4136

Dual LCD Backlight Inverter Drive IC

1. Description

Design goals for a CCFL inverter used in a notebook computer or portable applications include small size, high efficiency, and low cost. The FAN7548 provide the necessary circuit blocks to implement a highly efficient CCFL backlight power supply in a small footprint 20 SSOP package. The device features two control stages for operating independent resonant tanks for multi-lamp designs. It typically consumes less than 9mA of operating current, improving overall system efficiency. External parts count is minimized and system cost is reduced by integration such features as a feedback controlled PWM driver stage, the soft start, the open lamp regulation, the open lamp protection, the UVLO, and the self-synchronization circuitry between the buck and Royer stages.

They include an internal shunt regulator, allowing them to operate with input voltage from 6 to 26V. They support analog and burst dimming modes of operation. The FAN7548 provides the open lamp regulation, and the open lamp protection. The former can be used to protect the transformer from over-voltage during start up or when an open lamp occurs. The transformer voltage is regulated with reducing duty cycle when an over-voltage is detected. The latter can be used to shut IC down when an open lamp condition continue for more than a specific time.

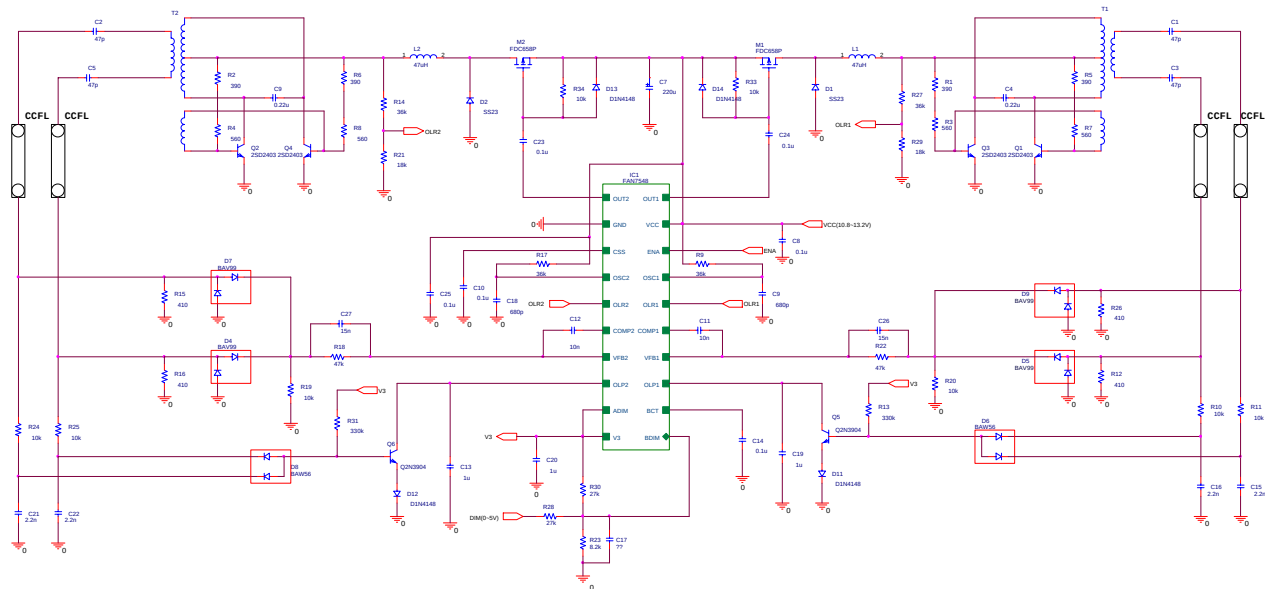


Figure 1. Application Circuit

2. Block Diagram and Basic Operation

2-1 Block Diagram

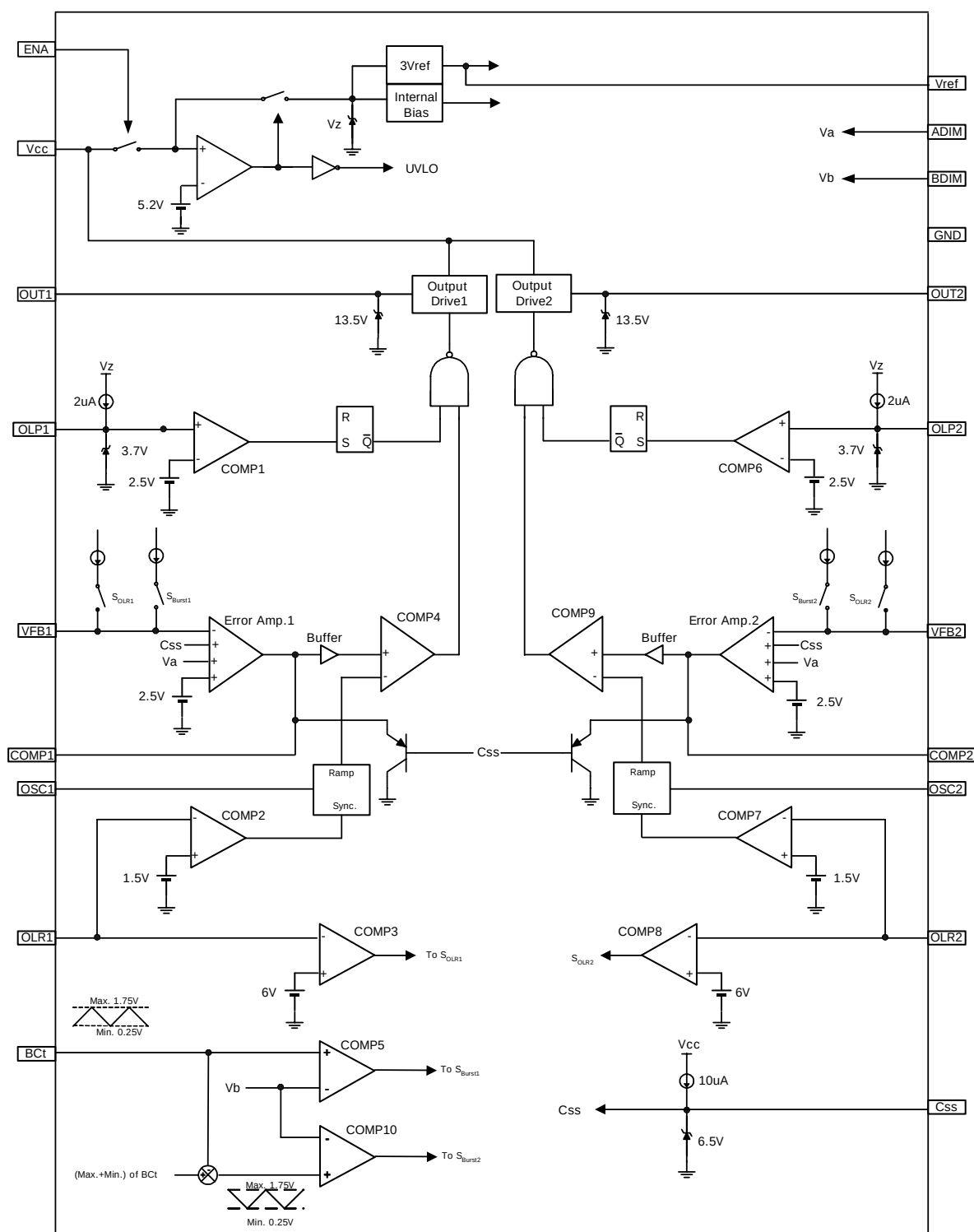


Figure 2. Block Diagram

2-2 Under Voltage Lockout (UVLO)

The under voltage lockout (UVLO) circuit (Figure 3) guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the V_{CC} value (Figure 4). The UVLO circuit turns on the control circuit when V_{CC} exceeds 5.4V. When V_{CC} is lower than 5.4V, the IC's standby current is less than 100uA. During UVLO, OLP, C_{SS} , and OSC pin is actively pulled low.

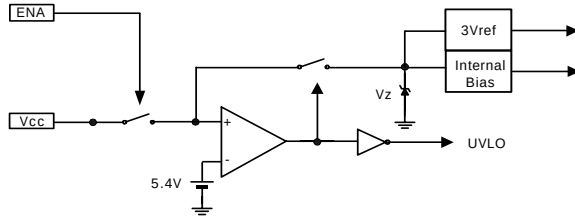


Figure 3. Under Voltage Lockout Circuit

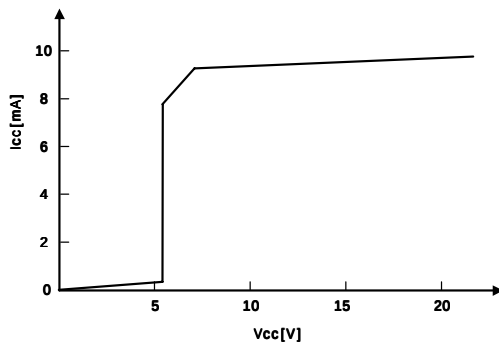


Figure 4. Start Voltage & Operating Current

2-3 Soft Start

The soft start function is provided with a capacitor connected to C_{SS} pin. The soft start time isn't related to the striking time for the CCFL. A soft start circuit ensures a gradual increase in the input and output power.

The C_{SS} capacitor determines the rate of rise of the voltage on C_{SS} pin, limiting COMP voltage, where the voltage level determines the on-time duration of buck stage's PMOSFET. It is charged by a current source of 10uA.

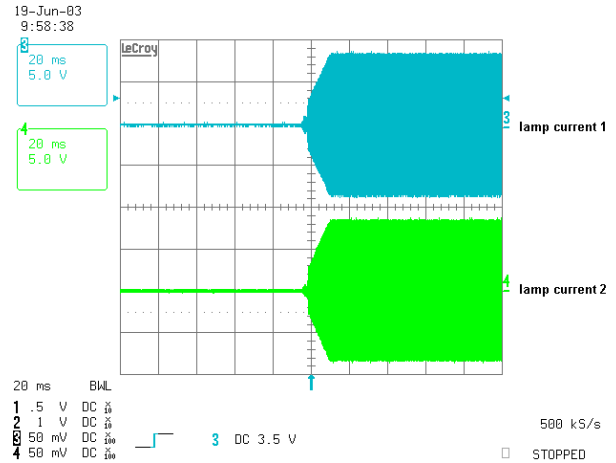
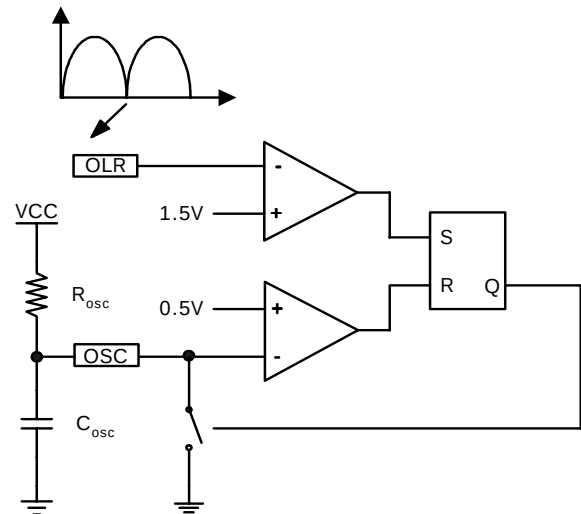


Figure 5. Soft Start During Initial Operation

2.4 Oscillator

1) Main Oscillator

A timing capacitor C_{OSC} is charged by a current source, formed by the timing resistor R_{OSC} , connected to the device's supply voltage. The exponentially shaped waveform charges up until OLR voltage goes through 1.5V downward. Then the capacitor begins discharging down to 0.5V. Next timing capacitor starts charging again. A new switching cycle begins. The frequency of OSC is synchronized with twice the tank resonant frequency and its maximum amplitude can be programmed with adjusting the values of R_{OSC} and C_{OSC} .



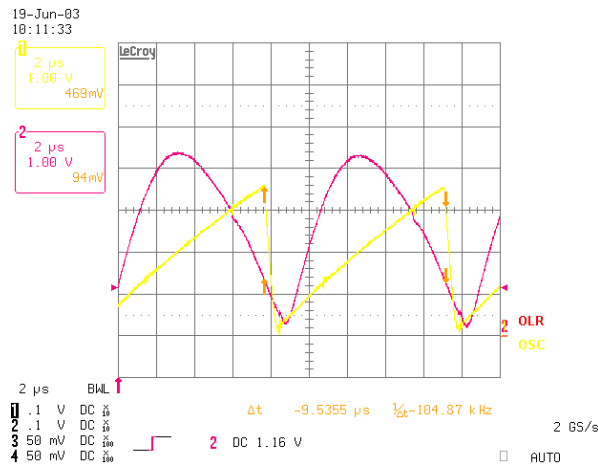


Figure 6. Main Oscillator Circuit & Waveform

2) Burst dimming oscillator

Timing capacitor BC_t is charged by 50uA. The triangular waveform charges up to 1.75V. Once reached, the capacitor begins discharging down to 0.25V. Next timing capacitor starts charging again and a new switching cycle begins. The burst dimming frequency can be programmed with adjusting the values of BC_t . The burst dimming frequency can be calculated as below

$$F_{\text{burst}} = \frac{50 \cdot 10^{-6}}{3 \cdot BC_t}$$

The burst dimming frequency should be greater than 120Hz to avoid visible flicker.

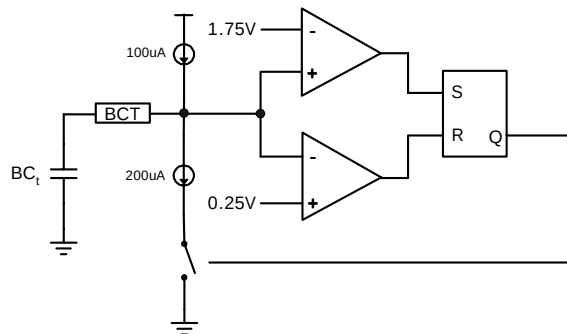


Figure 7. Burst Dimming Oscillator Waveform

2.5 Analog dimming

Lamp intensity is controlled with the signal ADIM. 2.5V on ADIM commands full brightness. Analog dimming waveforms are shown in Figure 8, 9, 10.

2.6 Burst dimming

Lamp intensity is controlled with the signal BDIM. 1.75V on BDIM commands full brightness. The duty cycle of the burst dimming comparator determines the lamp brightness as a percent of rated lamp current.

Burst dimming is implemented by summing 100uA into the feedback node to turn the lamp off. If there is sufficient voltage for lamp to strike, the feedback loop controls the lamp at rated current using a fixed current sense resistor. When the voltage of VFB is brought higher than V_{ref} , the COMP is low and the MOSFET stops switching.

The resonant tank voltage decays until the lamp extinguishes. CFB is reduced, if possible, to speed up the lamp re-strike. Burst dimming waveforms are shown in Figure 11, 12, 13.

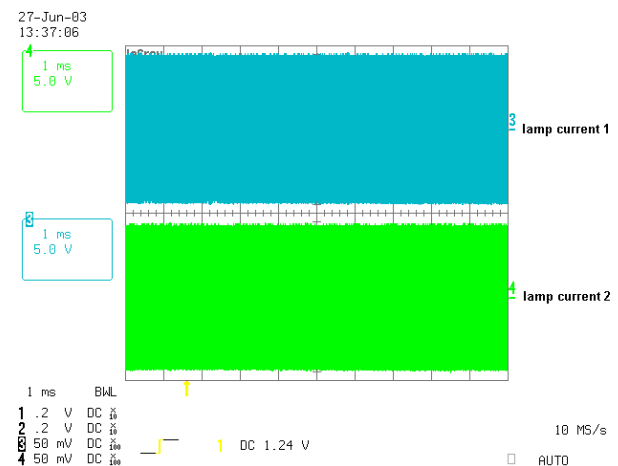


Figure 8. Analog Dimming at 100%

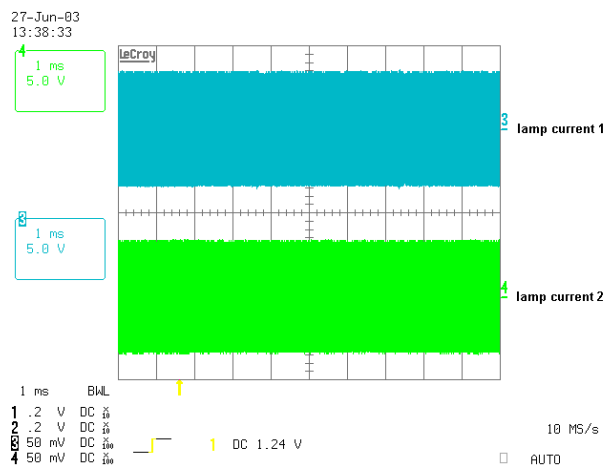


Figure 9. Analog Dimming at 50%

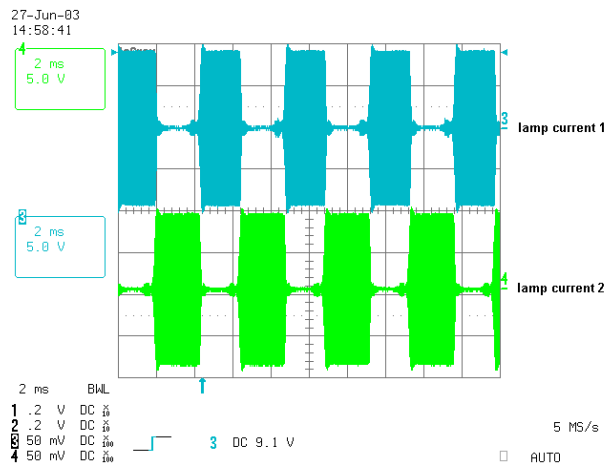


Figure 12. Burst Dimming at 50%

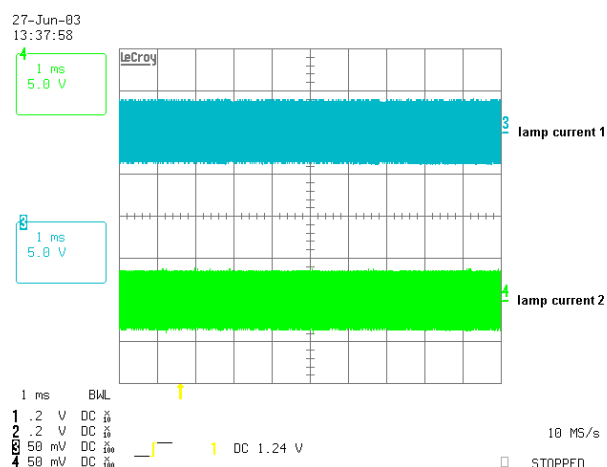


Figure 10. Analog Dimming at 25%

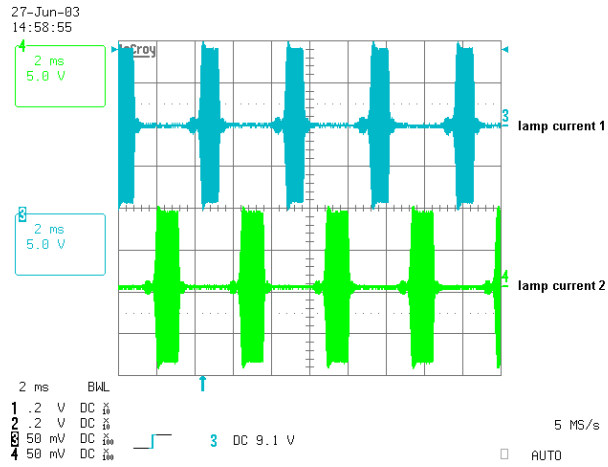


Figure 13. Burst Dimming at 25%

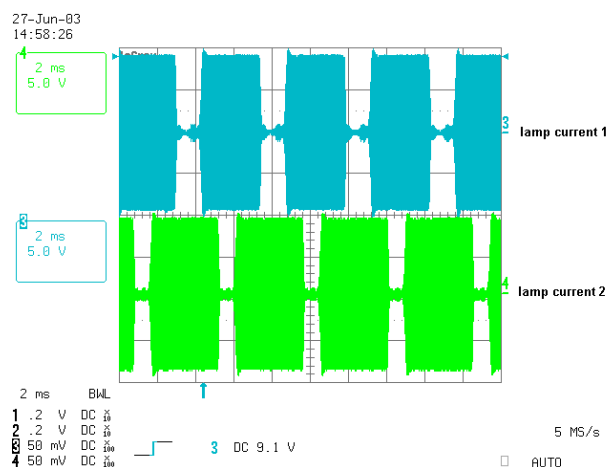


Figure 11. Burst Dimming at 75%

2.7 Open Lamp Regulation & Open Lamp Protection

It is necessary to suspend power stage operation if an open lamp occurs, because the power stage has high gain. When a voltage higher than 7.4V is applied to the OLR pin, the part enters the regulation mode and controls COMP voltage to limit the lamp voltage by summing 400uA into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 2.5uA internal current source. Once reached to 2.5V, IC enters shut down where the oscillator is inactive and output is high. In this mode, it draws little current at the V_{CC} pin and the OLP pin.

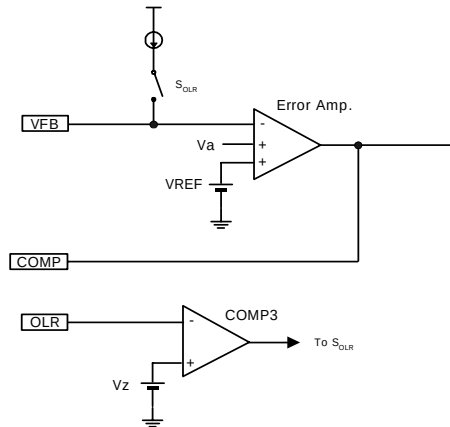


Figure 14. Open Lamp Regulation Circuit

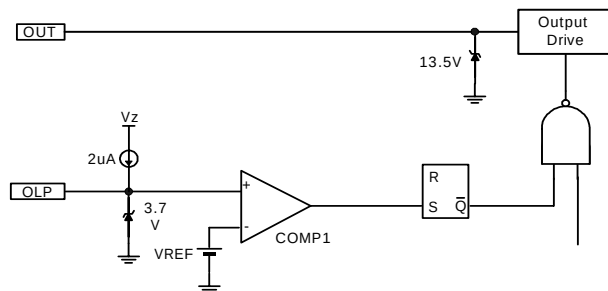


Figure 15. Open Lamp Protection Circuit

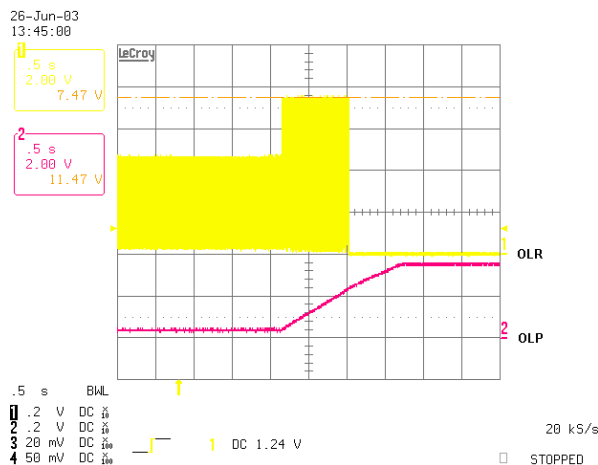


Figure 16. OLR Voltage During Open Lamp

3. Power Stage Design

Circuit operation

A current fed Royer topology is used to power the CCFL backlight shown in Figure 17. This topology accommodates a wide input voltage and dimming range while retaining sinusoidal operation of the lamp.

The converter consists of a resonant Royer stage, a high voltage output stage, and a buck stage used to regulate current in the converter.

Referring to Figure 17, the Royer stage consists of C_{res} , Q_1 , Q_2 , R_b , T_1 's primary and auxiliary windings.

The output stage consists of $C_{ballast}$, the lamp current sense resistor R_s , and T_1 's secondary. The resonant frequency of the tank is set by the primary inductance of T_1 , along with the resonant capacitor, C_{res} , and the reflected secondary impedance. The secondary impedance includes the lamp, the ballast capacitor, $C_{ballast}$, the distributed winding capacitance of T_1 , and the stray capacitance which forms between the lamp, lamp wires, and the backlight reflector. Since the lamp impedance is nonlinear with operating current, the tank resonant frequency will vary slightly with load.

The resonant tank consisting of C_{res} and T_1 produces sinusoidal currents, I_{res} , and voltages and is fed by a controlled DC current, I_{buck} , from the buck stage.

Note that the center tap voltage of the transformer is one half of the primary tank voltage. The high turns ratio transformer, T_1 , amplifies the sinusoidal tank voltage to produce a sinusoidal secondary voltage that is divided between the lamp and ballast capacitor.

Transistor Q_1 and Q_2 are driven out of phase at 50% duty cycle with an auxiliary winding on T_1 . The winding provides a floating AC voltage source at the resonant frequency that is used to drive the transistor bases alternately on and off.

The transistors channel the buck inductor current into opposing ends of the tank at the resonant frequency, supplying energy for the lamp and system losses.

The buck stage consists of inductor L_{buck} , MOSFET switch S_{buck} , and freewheeling diode D_{buck} .

In order to prevent interactions between multiple switching frequencies, the FAN7548 synchronizes the buck stage's frequency to the frequency of the Royer stage.

Lamp current is sensed directly with R_s and rectifying diode on each half cycle. The resulting voltage across the sense resistor R_s is kept at a V_{ref} (dependant on a selected dimming mode) average by the error amplifier, which in turn controls the duty cycle of S_{buck} .

The buck stage typically operates in continuous current mode but can operate with discontinuous current as the CCFL is dimmed.

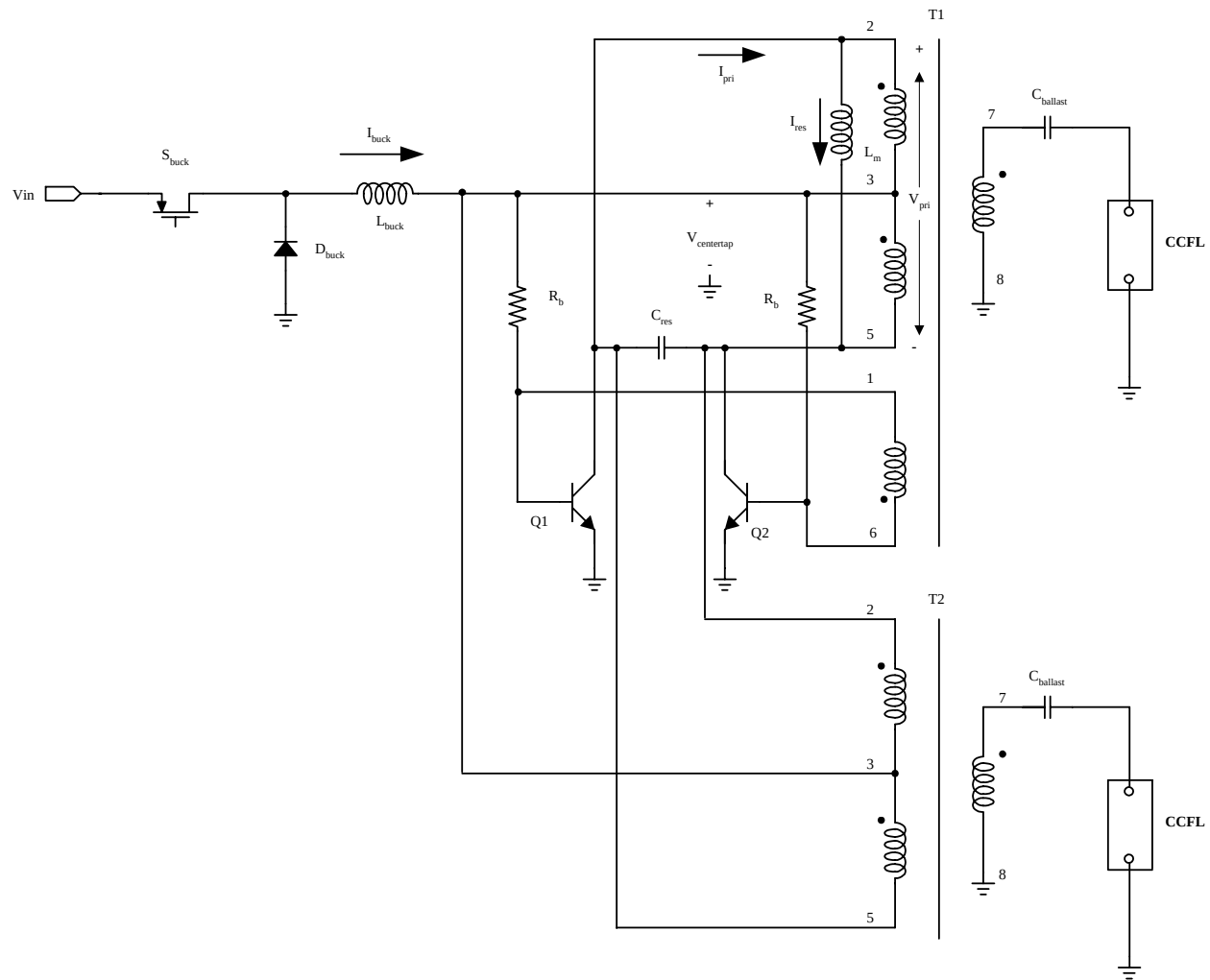


Figure 17. Power Stage of Driving Dual CCFLs

Design Procedure

A LCD monitor backlight circuit will be presented here to illustrate a design based on the FAN7548. The converter will be designed to drive two CCFLs with the following specifications.

Panel Model	LM151X2(LG.PHILIPS LCD)
Striking voltage	880V _{rms}
Operating voltage	585V _{rms} (Typ.)
Operating current	8mA _{rms} (Typ.)
Operating frequency	50kHz(Typ.)
Rated power	4.68W/CCFL

uInput voltage range :

The LCD monitor will be powered by a power source with an operational voltage range of 12V±10%.

Transformer's turns ratio selection & lamp striking voltage.

Before the lamp is struck, it presents impedance much larger than the ballast capacitor and the full output voltage of the transformer secondary is across the lamp.

Since the buck stage must reverse the volt-seconds on the buck inductor, the average tank voltage at the primary can be no greater than the DC input voltage.

This constraint along with the turns ratio of the royer transformer sets the maximum voltage available to strike the lamp.

The buck output voltage as a function of time can be as follows:

$$\begin{aligned}
 V_{\text{centertap}}(t) &= \frac{V_{\text{pri}}}{2} \cdot \sin \omega t \text{ where} \\
 &= 2 \cdot \pi \cdot f = \frac{2 \cdot \pi}{2 \cdot t_1} = \frac{\pi}{t_1} \\
 \int_0^{t_{\text{on}}} V_L(t) \cdot dt &= - \int_{t_{\text{on}}}^{t_1} V_L(t) \cdot dt \\
 \int_0^{t_{\text{on}}} \left(V_{\text{in}} - \frac{V_{\text{pri}}}{\sqrt{2}} \cdot \sin \omega t \right) \cdot dt &= - \int_{t_{\text{on}}}^{t_1} - \frac{V_{\text{pri}}}{\sqrt{2}} \cdot \sin \omega t \cdot dt \\
 \int_0^{t_{\text{on}}} V_{\text{in}} \cdot dt &= \int_0^{t_1} \frac{V_{\text{pri}}}{\sqrt{2}} \cdot \sin \omega t \cdot dt \\
 V_{\text{in}} \cdot t_{\text{on}} &= \frac{V_{\text{pri}}}{\sqrt{2}} \cdot -\cos \omega t \Big|_0^{t_1} = \frac{V_{\text{pri}}}{\sqrt{2}} \cdot \frac{2 \cdot t_1}{\pi} \\
 V_{\text{pri}} &= \frac{\pi}{\sqrt{2}} \cdot V_{\text{in}} \cdot D
 \end{aligned}$$

Condition 1) Minimum turns ratio, N_{min} to strike the lamp.

$$\begin{aligned}
 V_{\text{strike}} &= \frac{N_{\text{min}} \cdot \pi \cdot V_{\text{input, min}}}{\sqrt{2}} \\
 N_{\text{min}} &= \frac{\sqrt{2} \cdot V_{\text{strike}}}{\pi \cdot V_{\text{input, min}}} = \frac{\sqrt{2} \cdot 880}{\pi \cdot 10.8} \approx 37
 \end{aligned}$$

Condition 2) Minimum turns ratio, N_{min} to drive the lamp normally

$$\begin{aligned}
 V_{\text{sec}} &= \frac{N_{\text{min}} \cdot \pi \cdot V_{\text{input, min}}}{\sqrt{2}} \\
 N_{\text{min}} &= \frac{\sqrt{2} \cdot V_{\text{sec}}}{\pi \cdot V_{\text{input, min}}} = \frac{\sqrt{2} \cdot 1308}{\pi \cdot 10.8} \approx 54
 \end{aligned}$$

The transformer provided on the board has an 80:1 turns ratio, relating the entire secondary turns ratio to the primary. A minimum input of 10.8V will provide 1900V_{rms} to strike the lamp. If a higher striking voltage is required for the lamp, an increased transformer turns ratio, lower leakage transformer, or higher minimum input voltage is necessary.

Lamp voltage and ballast capacitor selection

The selection of components to be used in the resonant tank of the converter is critical in trading off the electrical and optical efficiencies of the system.

The value of the output circuit's ballast capacitor plays a key role in this trade-off. The voltage across the ballast capacitor can be expressed as function of the resonant frequency and secondary lamp current.

$$V_{\text{cb}} = \frac{I_{\text{lamp}}}{2 \cdot \pi \cdot C_{\text{ballast}} \cdot f_{\text{res}}}$$

A voltage drop across C_{ballast} many times the lamp voltage will make the secondary current insensitive to distortion caused by the nonlinear behavior of the lamp, providing a high impedance sinusoidal current source with which to drive the CCFL.

This approach improves the optical efficiency of the system, as capacitive leakage effects are minimized due to reduced harmonic content in the voltage waveforms.

Unfortunately, from an electrical efficiency standpoint, an increased tank voltage produces increased flux losses in the transformer and increased circulating currents in the tank. In practice, the voltage drop across the ballast capacitor is selected to be approximately twice the lamp voltage (1170V in our case) at rated lamp current.

Assuming a 50KHz resonant frequency and 8mA operating current, a ballast capacitance of 22pF is selected.

Since the lamp and ballast capacitor impedance are 90 degrees out of phase, the secondary voltage on the transformer is the following.

$$V_{\text{sec}} = \sqrt{V_{\text{cb}}^2 + V_{\text{lamp}}^2} = \sqrt{1170^2 + 585^2} \approx 1308V_{\text{rms}}$$

Since the capacitor dominates the secondary impedance, the lamp current maintains a sinusoidal shape despite the nonlinear behavior of the lamp.

The value of ballast capacitor has no effect on current regulation since the average lamp current is sensed directly by the controller.

uResonant frequency & transformer's primary inductance selection

Once the ballast capacitor is selected, the resonant frequency of the Royer stage can be determined from the transformer's

inductance(L_p), turns ratio(N), the resonant capacitor(C_{res}) and the ballast capacitor($C_{ballast}$).

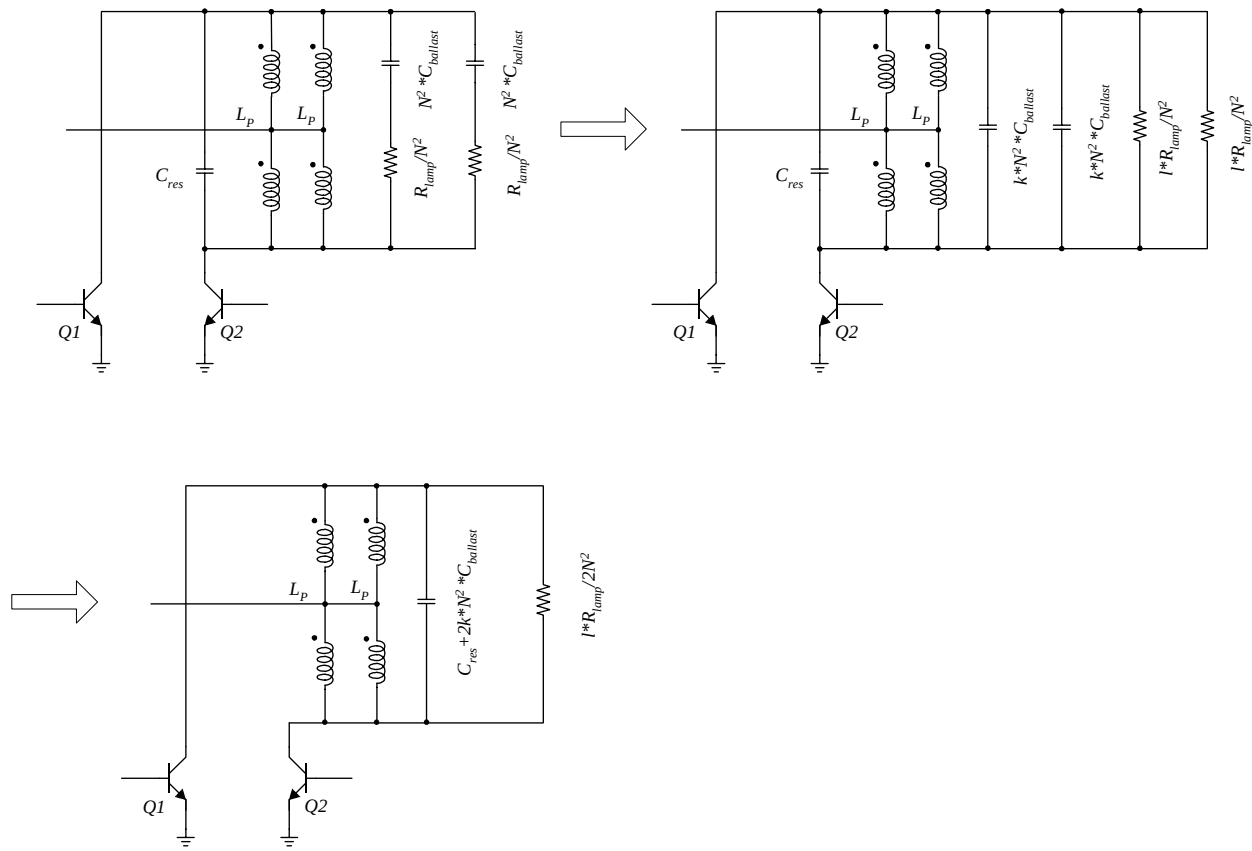


Figure 18. Equivalent Circuit of Power Stage

$$f_{res} = \frac{1}{2 \cdot \pi \cdot \sqrt{\frac{L_p}{2} (C_{res} + 2 \cdot k \cdot N^2 \cdot C_{ballast})}}$$

where k : conversion coefficient from a series circuit to parallel one

Output distortion is minimized by keeping the independent resonant frequencies of the primary and secondary circuits equal. This is achieved by making the resonant capacitor equal to the ballast capacitance times the turns ratio squared.

$$C_{res} = 2 \cdot N^2 \cdot C_{ballast} = 2 \cdot 80^2 \cdot 22\text{pF} \approx 0.28\mu\text{F} \Rightarrow 0.27\mu\text{F}$$

The resulting resonant frequency is about 50kHz, but this frequency will vary depending upon the lamp load and amount of stray capacitance in the system. It is important that the operating frequencies of a particular design are within the synchronizable frequencies of the controller.

$$C_R = C_{res} + 2 \cdot k \cdot N^2 \cdot C_{ballast} \\ = 0.27\mu\text{F} + \frac{2 \cdot 80^2 \cdot 22\text{pF}}{1.25} \approx 0.495\mu\text{F}$$

$$L_p = \frac{2}{(2 \cdot \pi \cdot f_{res})^2 \cdot C_R} = \frac{2}{(2 \cdot \pi \cdot 50 \cdot 10^3)^2 \cdot 0.495 \cdot 10^{-6}} \approx 41\mu\text{H}$$

Primary and secondary RMS currents are then calculated to determine maximum acceptable transformer winding resistances. The secondary current is mostly lamp current, although the currents to drive distributed winding and stray wiring capacitances are also factors. For now we will ignore these parasitic effects, since in most cases the additional loss they cause will not be enough to significantly alter the transformer design.

Each half of the primary winding sees an asymmetrical sinusoidal current which is the sum of the primary resonant current, the reflected secondary lamp current, and the input current source from the buck stage during one-half of the cycle. The primary voltage must be calculated first in order to determine the primary resonant current.

$$V_{pri} = \frac{N_p}{N_s} \cdot V_{sec} = \frac{N_p}{N_s} \cdot \sqrt{V_{cb}^2 + V_{lamp}^2}$$

$$= \frac{1}{80} \cdot \sqrt{1170^2 + 585^2} \approx 16.35 V_{rms}$$

The primary resonant current on each transformer is then

$$I_{res} = \frac{V_{pri}}{\sqrt{\frac{L_p}{C_{res}}}} \cdot \sqrt{1 + \frac{k \cdot N^2 \cdot C_{ballast}}{C_{res}}}$$

$$= \frac{16.35}{\sqrt{\frac{41}{0.135}}} \cdot \sqrt{1 + \frac{k \cdot N^2 \cdot C_{ballast}}{C_{res}}} \approx 1.26 A_{rms}$$

Average inductor current of buck stage is calculated by equating input and output power assuming 90% efficiency for the Royer stage.

$$P_{in} = \frac{P_{out}}{0.9} = \frac{2 \cdot V_{lamp,rms} \cdot I_{lamp,rms}}{0.9} = \frac{2 \cdot 585 \cdot 0.008}{0.9} \approx 10.4 W$$

The buck stage sources current to the Royer stage through the primary winding's center tap. The average voltage at this point is one-half of the total primary voltage.

The average buck stage output voltage is therefore one-half the average primary voltage calculated

$$V_{buck} = \frac{\sqrt{2} \cdot V_{pri}}{\pi} = \frac{\sqrt{2} \cdot 16.35}{\pi} \approx 7.36 V_{dc}$$

The buck output current is then:

$$I_{buck} = \frac{P_{in}}{V_{buck}} = \frac{10.4}{7.36} \approx 1.41 A_{dc}$$

The primary current on each transformer consists of the primary resonant current, the reflected secondary lamp current to the primary side and I_{buck} .

$$I_{pri,peak} = \sqrt{2} \cdot I_{res} \cdot \sin\left(\omega t - \frac{\pi}{2}\right) + \sqrt{2} \cdot N \cdot I_{lamp}$$

$$\cdot \sin(\omega t + \theta) + \frac{I_{buck}}{2}$$

$$I_{pri} = \sqrt{\frac{1}{2\pi} \cdot \int_0^{2\pi} I_{pri,peak}^2 d(\omega t)}$$

$$= \sqrt{I_{res}^2 + N^2 I_{lamp}^2 + \left(\frac{I_{buck}}{4}\right)^2 - 2 \cdot I_{res} \cdot N \cdot I_{lamp} \cdot \sin \theta}$$

$$\approx 0.82 A_{rms}$$

$$\text{where } \theta = \tan^{-1}\left(\frac{X_{cb}}{R_{lamp}}\right)$$

Buck Stage Design

The Royer converter's resonant frequency establishes the buck stage's conversion frequency. Each time the Royer converter's primary voltage crosses through zero, the FAN7548's oscillator is reset.

The design frequency for the buck stage is therefore twice Royer resonant frequency.

The buck stage provides a regulated, variable output voltage for the Royer converter to reject input voltage variations and allow lamp brightness adjustment.

Due to the absence of a large output capacitor, the buck stage presents a high impedance to the Royer converter at its resonant frequency. Neglecting the sawtooth ripple, the output inductor's current is nearly constant.

Inductor ripple current is greatest when the duty cycle and frequency are minimum. This occurs at maximum input voltage and lamp current, where off time is maximum.

$$T_{off,max} = \frac{1-D}{f_{min}} = \frac{1}{f_{min}} \left(1 - \frac{V_{buck}}{V_{in,max}}\right)$$

$$= \frac{1}{100 \cdot 10^3} \left(1 - \frac{7.36}{13.2}\right) \approx 4.24 \mu s$$

To minimize inductor value, ripple current is normally less than 50% of the maximum average value.

$$L > \frac{T_{off} \cdot V_{buck}}{I_{buck}} = \frac{T_{off} \cdot V_{buck}}{0.5 \cdot I_{buck}} = \frac{4.42 \mu \cdot 7.36}{0.5 \cdot 1.41}$$

$$\approx 46 \mu H$$

References

1. M. Jordan, J. O' Connor, "Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution", Unitrode application note U-141
2. J. O' Connor, "Dimmable Cold-Cathode Fluorescent Lamp Ballast Design Using The UC3871", Unitrode application note U-148
3. Abraham I. Pressman, "Switching Power Supplying Design", McGraw-Hill International

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